What is claimed is:

1. An image signal processing device, which converts input pixel data corresponding to each of the pixels of a display panel into an analog image signal, comprising:

a calculation portion for adding high-order bit pixel data to a value corresponding to the least significant bit digit in said high-order bit pixel data to obtain addition high-order bit pixel data, said high-order bit pixel data being constituted by high-order consecutive bits of said input pixel data;

a selection portion for selecting either said addition high-order bit pixel data or said high-order bit pixel data in accordance with a value of low-order bit pixel data, said low-order bit pixel data being constituted by low-order consecutive bits of said input pixel data; and,

a D/A conversion portion for performing digital-to-analog conversion of the selected pixel data to obtain said analog image signal.

2. An image signal processing device according to Claim 1, wherein said selection portion selects said addition high-order bit pixel data during a time period corresponding to value of said low-order bit pixel data in a prescribed unit period, and selects said high-order bit pixel data during other period in said prescribed unit period.

3. An image signal processing device according to Claim 1, wherein said low-order bit pixel data comprises low-order consecutive M bits (M is a natural number) of said input pixel

data, and in image signal processing of each consecutive 2^M frame's worth of said input pixel data, said selection portion selects said addition high-order bit pixel data for frames corresponding in number to a value of said low-order bit pixel data, and selects said high-order bit pixel data for the other frames.

4. An image signal processing device according to Claim 1, wherein said low-order bit pixel data comprises low-order consecutive M bits including the least significant bit of said input pixel data comprising N-bit (N is a natural number, and M is a natural number smaller than N), and said high-order bit pixel data comprises high-order consecutive (N-M) bit including the most significant bit of said input pixel data.

5. An image signal processing device, which converts input pixel data corresponding to each of the pixels of a display panel into an analog image signal, comprising:

a D/A conversion portion for performing digital-to-analog conversion processing of high-order bit pixel data comprising high-order consecutive bits in said input pixel data to obtain an analog signal; and,

a calculation portion for outputting an addition result, as said analog image signal, of said analog signal and a value corresponding to the least significant bit digit in said high-order bit pixel data in accordance with a value of low-order bit pixel data, said low-order bit pixel data being constituted by low-order consecutive bits of said input pixel data.

6. An image signal processing device according to Claim 5, wherein said calculation portion outputs said addition result as said analog image signal during a time period corresponding to a value of said low-order bit pixel data in a prescribed unit period and outputs said analog signal as said analog image signal during other time period in said prescribed unit period.

7. An image signal processing device according to Claim 5, wherein said low-order bit pixel data comprises low-order consecutive M bits (M is a natural number) of said input pixel data, and in image signal processing of each consecutive 2^M frame's worth of said input pixel data, said calculation portion outputs said addition result as said analog image signal for frames corresponding in number to a value of said low-order bit pixel data, and outputs said analog signal as said analog image signal for the other frames.

8. An image signal processing device according to Claim 5, wherein said low-order bit pixel data comprises low-order consecutive M bits including the least significant bit of said input pixel data comprising N bits (N is a natural number, and M is a natural number smaller than N), and said high-order bit pixel data comprises high-order consecutive (N-M) bits including the most significant bit of said input pixel data.